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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,669	09/30/2003	Dave Stumbo	2132.0080001	2029

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NANOSYS INC.
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EXAMINER	
LIANG, REGINA	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,669	STUMBO ET AL.	
	Examiner	Art Unit	
	Regina Liang	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3-42, 44-50, 52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-42, 44-50, 52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to the amendment filed on 7/1/05. Claims 1, 3-42, 44-50, 52 are pending in this application.

Claim Rejections - 35 USC 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-42, 44-49, 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art (Figs. 1, 2 and sections [0003]-[0008], hereinafter the admitted prior art) in view of Koyama et al (US. PUB. NO. 2002/0024489 hereinafter Koyama) and Avouris et al (US. PUB. NO. 2004/0061422 hereinafter Avouris).

As to claim 1, Figs. 1 and 2 of the admitted prior art discloses an active matrix backplane used within a display, comprising a plurality of pixels, a plurality of pixel transistors. The admitted prior art does not disclose each pixel transistor is a nanowire transistor and comprises a plurality of nanowires extending between a first source electrode and a first drain electrode of the transistor. However, it is well known in the art that an active matrix display having a plurality of pixels and using field-effect transistors (for instance, thin-film transistors) as the switching elements (e.g., see Koyama [0039]). It is also old and well known in the art that a field-effect transistor comprising a nanowire transistor, and the nanowire transistor comprising a plurality of nanowires extending between a first source electrode and a first drain electrode of the transistor

(see Avouris on page 2, sections [0032], [0033], and [0035]). Thus, in view of the teachings of Koyama and Avouris, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the pixel transistor of the admitted prior art to be a field-effect transistor comprising nanowires transistor as taught by Avouris since the nanowires forming the channel region is made very small such that the space requirement on a chip area is reduced.

As to claims 4, 7, 27, 32, 52, Fig. 2 of the admitted prior art teaches the matrix backplane comprising a plurality of column transistors and a plurality of row transistors. Avouris teaches the transistor comprising a nanowire transistor. Thus it would have been further obvious to one of ordinary skill in the art at the time the invention was made to modify the column transistors and the row transistors of admitted prior art to be nanowire transistors as claimed since the nanowire forming the channel region is made very small such that the space requirement on a chip area is further reduced.

As to claims 5, 8, Avouris teaches the nanowire transistor comprising nanowires extending at least between a source and a drain electrode.

As to claims 10-13, 28-31, to further use nanowire technology to make the related components as claimed would have been further obvious to one of ordinary skill in the art since it would further reduce the size of the overall device on a chip area.

As to claims 14-26, the admitted prior art teaches the display is LCD, OLED, etc as claimed ([0003]).

As to claims 33-36, see section [0009] of the admitted prior art.

As to claims 3, 6, 9, 37-42, 44-49, the admitted prior art as modified by Koyama and Avouris discloses the claimed invention except for the arrangement, location, value and material

of the nanowires transistors. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the admitted prior art as modified by Koyama and Avouris to have the nanowires transistors as claimed, since it has been held that discovering an optimum value, range, location, material of a result effective variable involves only routine skill in the art.

4. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art (Figs. 1, 2 and sections [0003]-[0008], hereinafter the admitted prior art) in view of Koyama et al (US. PUB. NO. 2002/0024489 hereinafter Koyama) and Roesner et al (US. PAT. NO. 2003/0132461 hereinafter Roesner)

As to claim 50, Figs. 1 and 2 of the admitted prior art discloses an active matrix backplane used within a display, comprising a plurality of pixels, a plurality of pixel transistors. The admitted prior art does not disclose each pixel transistor is a nanowire transistor and comprises a plurality of nanowires extending between a first source electrode and a first drain electrode of the transistor. However, it is well known in the art that an active matrix display having a plurality of pixels and using field-effect transistors (for instance, thin-film transistors) as the switching elements (e.g., see Koyama [0039]). It is also old and well known in the art that a field-effect transistor comprising a non-nanotube nanowire transistor, and the non-nanotube nanowire transistor comprising a plurality of nanowires extending between a first source electrode and a first drain electrode of the transistor (see Roesner on page 2, section [0028], page 4 [0072]-[0078]). Thus, in view of the teachings of Koyama and Roesner, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the

pixel transistor of the admitted prior art to be a field-effect transistor comprising non-nanotube nanowires transistor as taught by Roesner since the nanowires forming the channel region is made very small such that the space requirement on a chip area is reduced.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 3-42, 44-50, 52 have been considered but are moot in view of the new ground(s) of rejection.

Applicants' remarks regarding Koyama and Avouris on pages 10-11 are not persuasive. Both applicants' admitted prior art and Koyama teach the transistors in the display matrix are used to control turn on and off by controlling the voltage or current applied to the corresponding pixels in the display. Avouris is used to teach a field-effect transistor can be fabricated through nano-technology by using nanoelement such as nanotube or nanowire in the circuit configuration to increase integration density of the components on a chip. Therefore, applicant' argument that light emitting device disclosed in Avouris is not used to control (turn on and off) the pixels of display are moot and not persuasive.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Regina Liang
Primary Examiner
Art Unit 2674

8/5/05